



2133
#4/a
KWS
6-12-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: JOHN S. SADOWSKY § Group Art Unit: 2133
Serial No.: 09/670,231 §
Filed: September 28, 2000 § Examiner: Anthony T. Whittington
For: A DECODER FOR TRELLIS-BASED CHANNEL ENCODING § Atty. Dkt. No.: INTL-0328-US (P8031)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RECEIVED
JUN 11 2003

REPLY TO PAPER NO. 3

Technology Center 2100

Sir:

In response to the Office Action mailed March 26, 2003, please amend the above-referenced patent application as follows:

In the Claims:

Please amend claims 1-4, 6-7, 9-12, 17-18, 21-22, 25 and 26 as follows:

- a
1. (Amended) A system comprising:
a digital signal processor comprising a bus connectable to a memory; and
a butterfly coprocessor coupled to the digital signal processor to perform an operation scheduled by the digital signal processor.
 2. (Amended) The system of claim 1, wherein the digital signal processor further comprises:

Date of Deposit: June 3, 2003
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Jennifer Juarez